DPDK
DATA PLANE DEVELOPMENT KIT

Enabling hardware acceleration in DPDK data-plane applicatio

DPDK Summit - San Jose – 2017

#DPDKSummit

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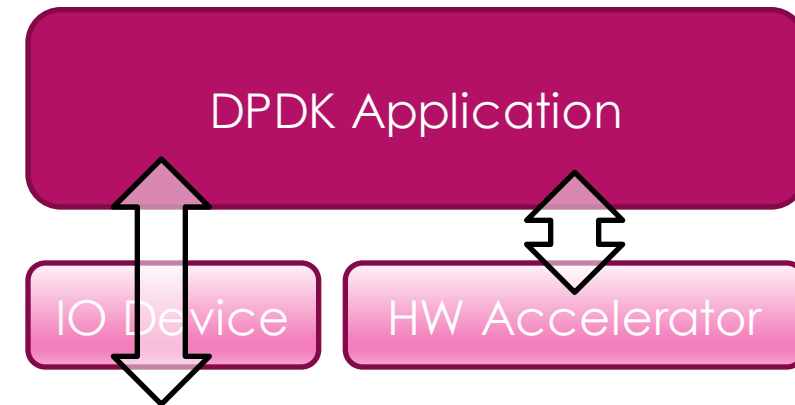
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Agenda

▶ Hardware Accelerations Models

▶ Applications Integration of hardware acceleration

▶ Agnostic API enablement and metadata propagation

▶ Future Challenges

DPDK

- ▶ Characteristics
  - ▶ Independent of platform IO.
  - ▶ Usually asynchronous in operations, enqueue/dequeue operation to the accelerator.
  - ▶ Can be either stateful or stateless.
- ▶ Common examples include:
  - ▶ Symmetric/asymmetric crypto, compression, event scheduling
- ▶ Any discrete, independent pipeline stage could be accelerated in this way

Platform Logical View

DPDK Application

IO Device | HW Accelerator

Application Pipeline View

Rx → PIPELINE STAGE → PIPELINE STAGE → PIPELINE STAGE → Tx

HW Acc.
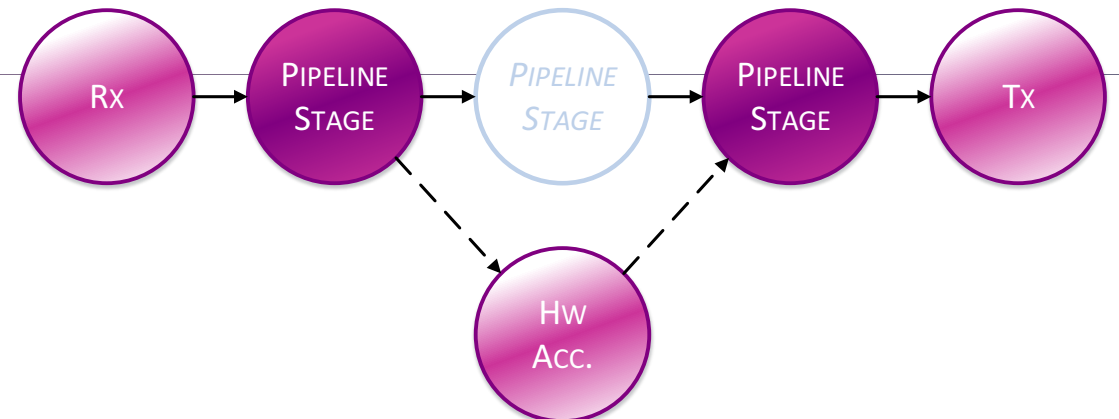
Inline IO Hardware Acceleration

- ▶ Characteristics
  - ▶ Integrated into IO hardware device
  - ▶ May generate metadata for host consumption.
  - ▶ May require metadata from host for successfully processing.
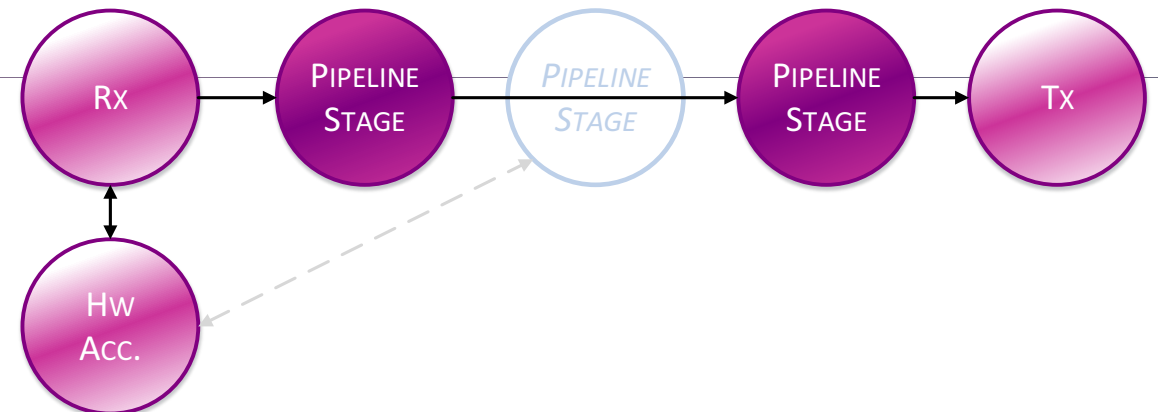 - ▶ Can be either stateful or stateless.
- ▶ Common examples include:
  - ▶ CRC, checksums, TSO, load distribution (Flow director/RSS)
  - ▶ Switching, inline crypto, hierarchical QoS

Platform Logical View

DPDK Application

IO Device   HWAcc.

Application Pipeline View

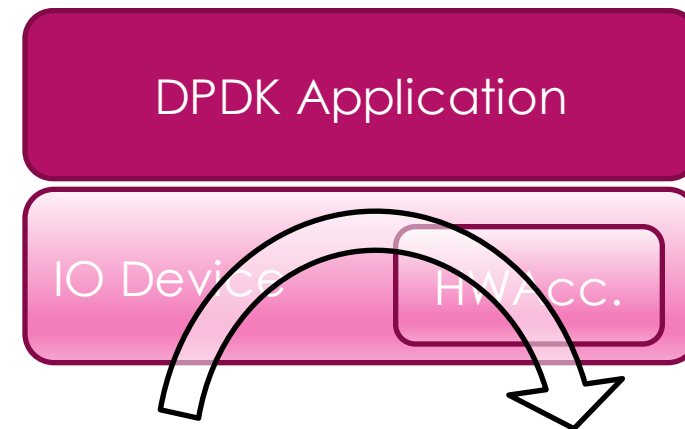Rx → Pipeline Stage → *Pipeline Stage* → Pipeline Stage → Tx

Hw Acc.
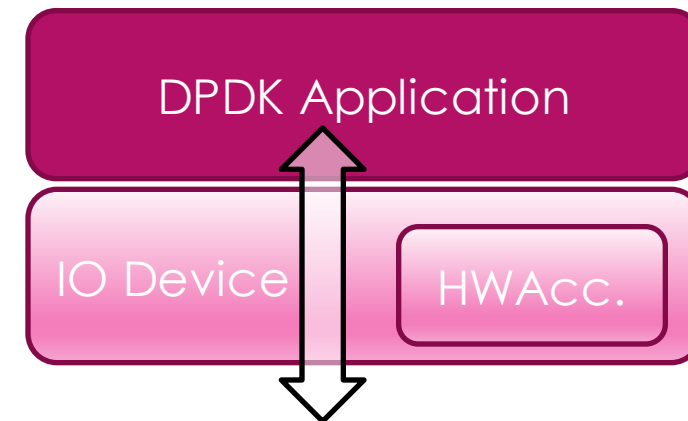
Full Pipeline Hardware Acceleration

DPDK
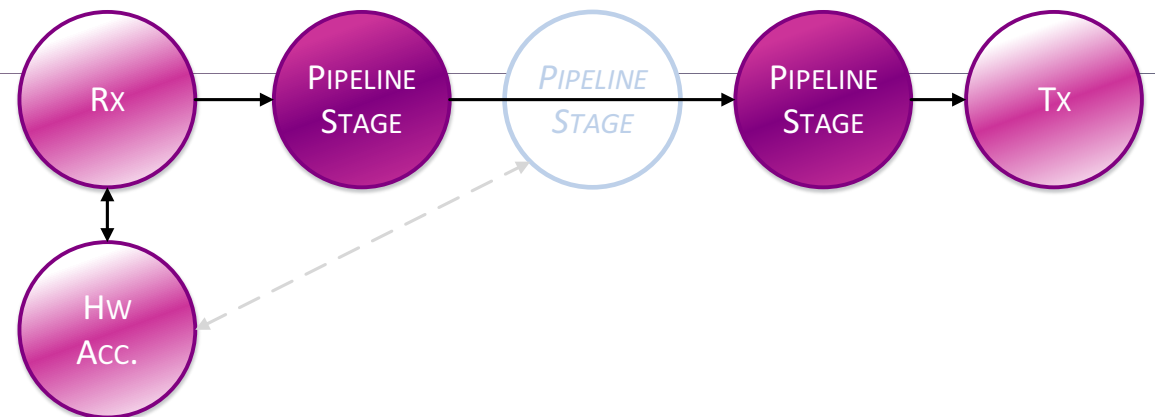
- Characteristics

  - Integrated into IO hardware device

  - All processing happens in the IO device.

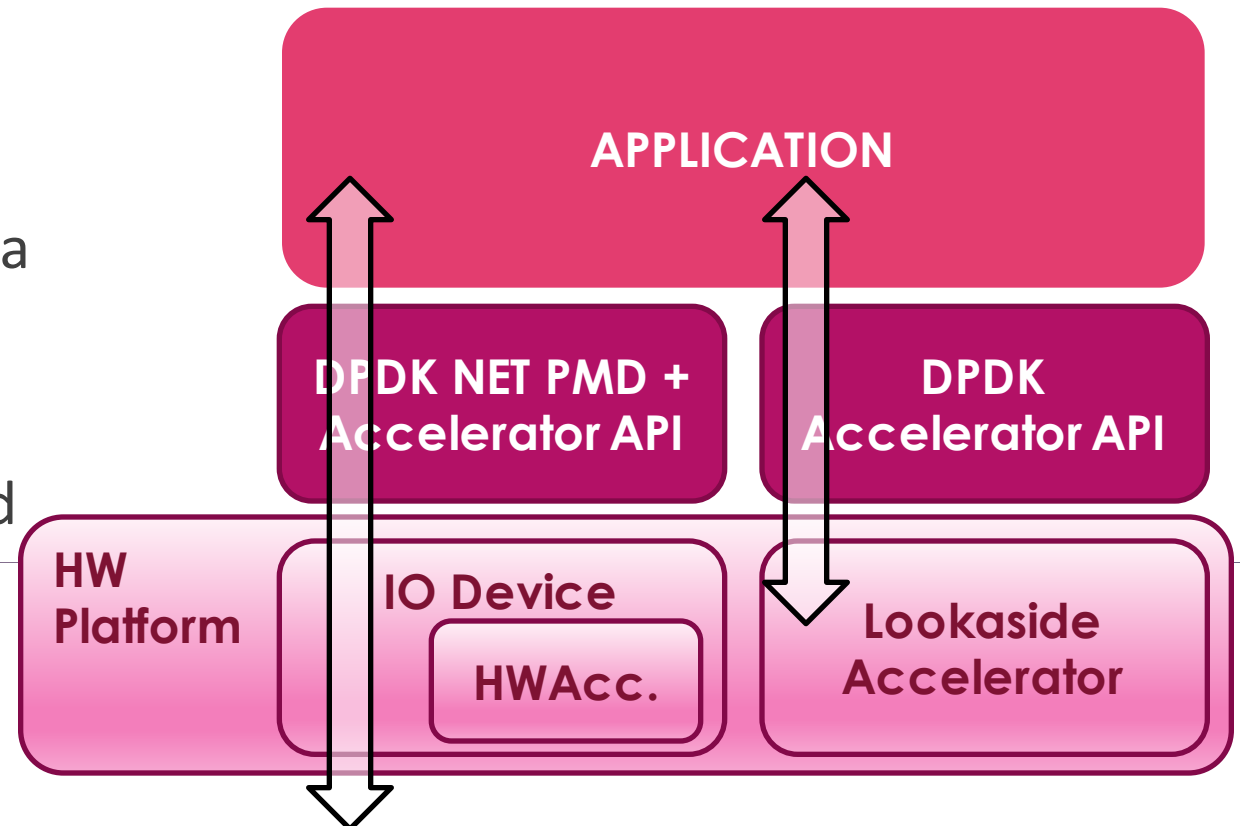 - Application only provides control plane/exception path.

Platform Logical View

DPDK Application

IO Device   HW Acc.

Application Pipeline View

Rx → PIPELINE STAGE → *PIPELINE STAGE* → PIPELINE STAGE → Tx

Hw Acc.

Appliance

- ▶ Appliance application is platform/accelerator aware.

- ▶ May be developed in a way which requires a particular acceleration as a prerequisite.

- ▶ Application has ownership of hardware acceleration resources and manages it's configuration.

APPLICATION

DPDK NET PMD + Accelerator API

DPDK Accelerator API

HW Platform

IO Device

HWAcc.

Lookaside Accelerator

NFVi/VNF

- ▶ Infrastructure application is platform/accelerator aware.

- ▶ Infrastructure application has ownership of hw acceleration resources and manages it's configuration.

- ▶ VNF application is unware of the platform infrastructure and infrastructure accelerations such as switching and TEP which are configured by the NFVi

VNF

VNF

NET PMD

NET PMD

Acc. API

NFVi Application (vswitch)

NET PMD / Acceleration API

HW Platform

IO Device
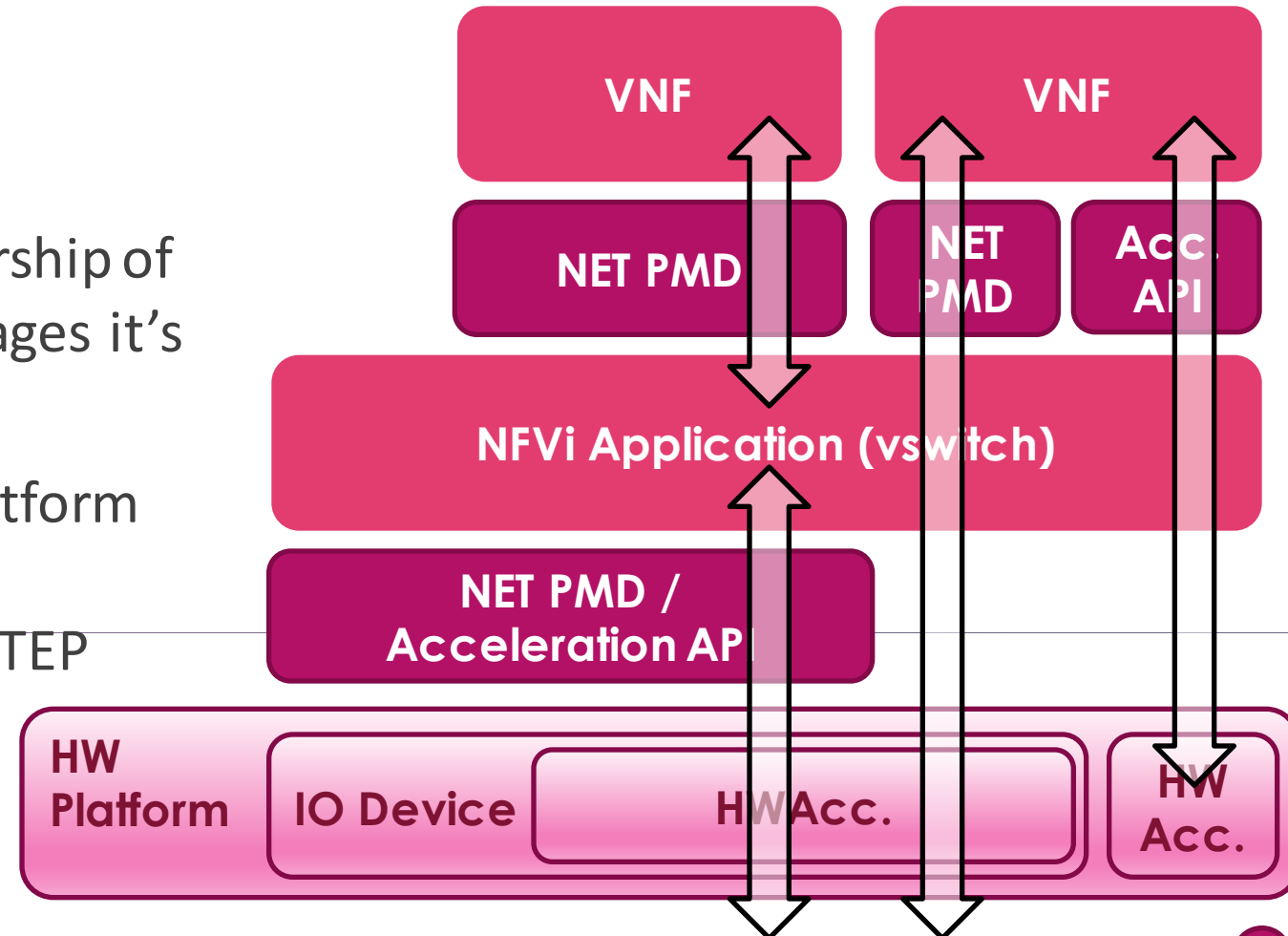
**HWAcc.**

HW Acc.

Key considerations for hw acceleration

▶ Understand the impact to the application architecture by using hw acceleration ie how is the application pipeline affected.

▶ Does the hardware acceleration support all scenarios or does the application need to handle exception cases in software.

▶ Does the hardware acceleration place restrictions on the application.

Hardware Acceleration of IPsec

▶ Many ways to accelerate IPsec data path processing.

　　▶ Lookaside crypto

　　▶ Lookaside protocol

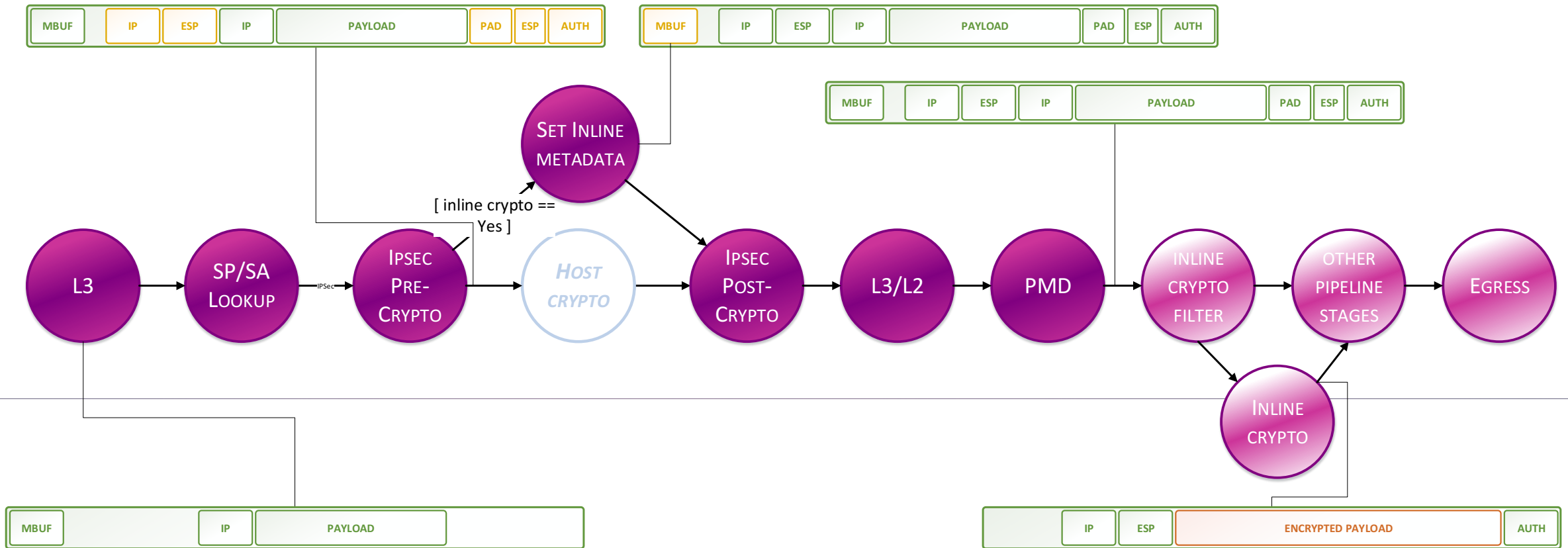　　▶ Inline crypto

　　▶ Inline protocol

IPsec lookaside crypto acceleration
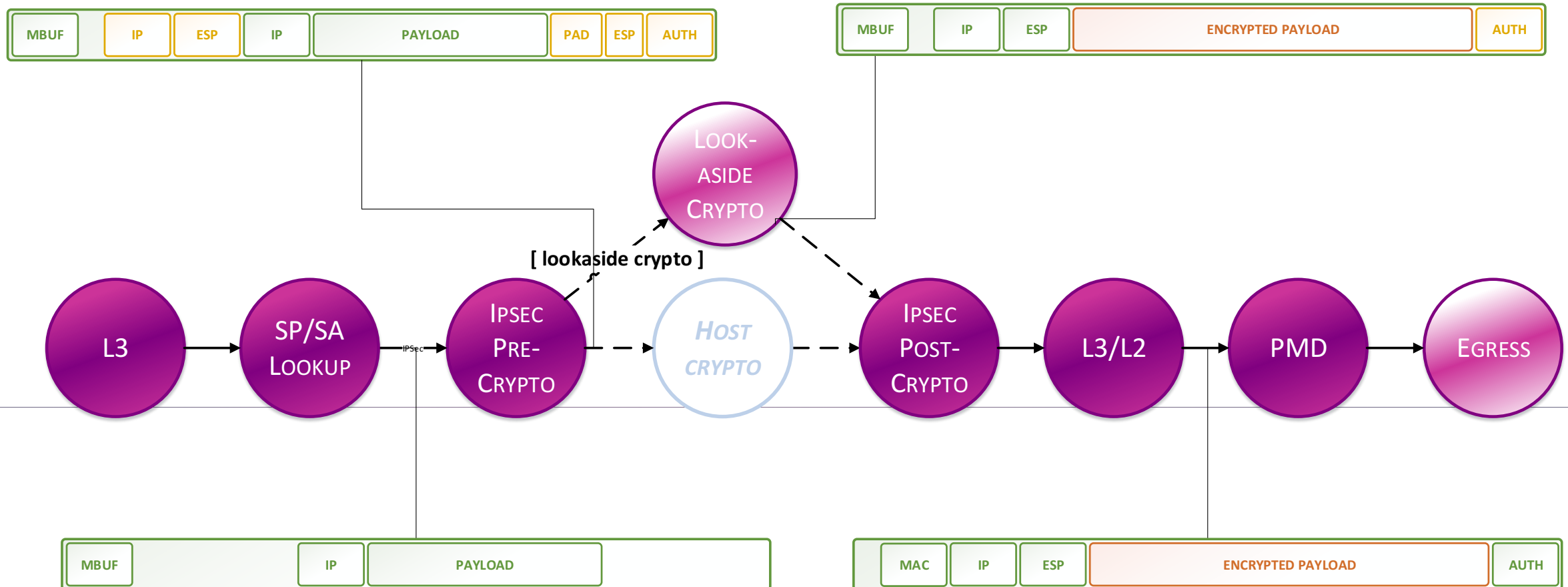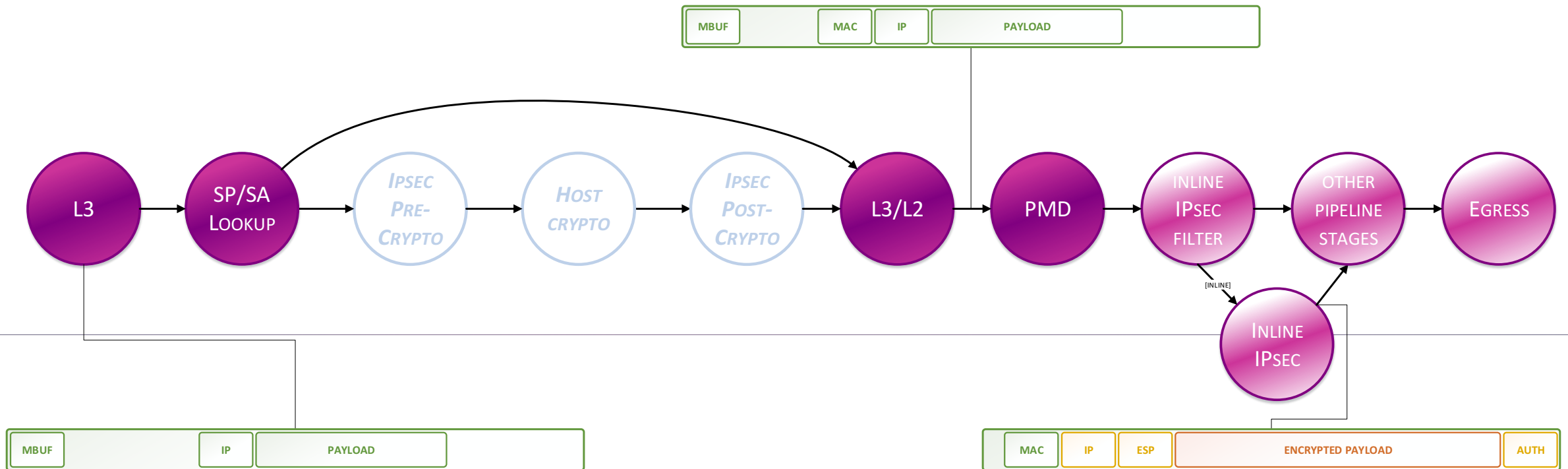
IPsec lookaside protocol acceleration
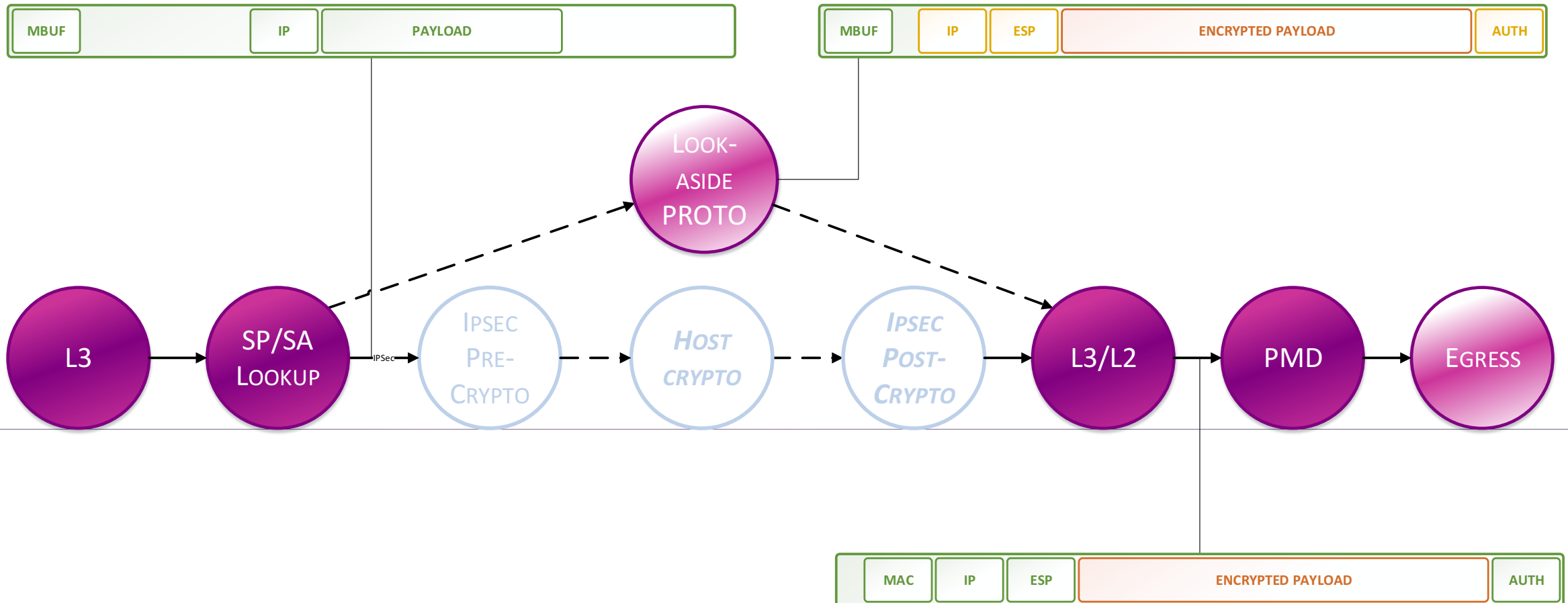
IPsec inline crypto acceleration

IPsec inline protocol acceleration

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Summary

▶ API must be driven by the functional feature and not a particular hardware implementation.

▶ features and capabilities must be dynamically discoverable, to enable the application to adapt it's control plane and it's data path processing pipeline.

▶ Need to allow applications to easily distinguish between packets which have been handled by the accelerator.

▶ For inline IO accelerations metadata is the glue to allow the application to discovery if packets have been processed inline or not.

    ▶ Allows applications to support hybrid solutions with both accelerated and non-accelerated simultaneously.

▶ Hardware Acceleration can introduce restrictions to the application architecture and pipeline.

Questions?

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